WE CLAIM:

1. A method of testing a multi-port memory in accordance with a test pattern, the memory including a set of access ports and a plurality of memory cells accessible through the access ports, the access ports including at least first and second ports, the test pattern including at least a test element that is to be performed upon each of the memory cells and that includes at least consecutive first and second memory operations, said method comprising:

a) generating a set of test clock signals that have the same test clock frequency, the test clock signals including at least a first test clock for controlling memory access through the first port, and a second test clock for controlling memory access through the second port, clock pulses of the second test clock lagging corresponding clock pulses of the first test clock by a first delay period; and

b) conducting the first and second memory operations in a folded sequence upon one of the memory cells during the same test clock cycle of the test element, wherein the first memory operation is conducted through the first port during a first time period starting from a leading edge of one of the clock pulses of the first test clock and ending at a lagging edge of said one of the clock pulses of the first test clock, and wherein the second memory operation is conducted through the second port

during a second time period starting from a leading edge of one of the clock pulses of the second test clock and ending at a lagging edge of said one of the clock pulses of the second test clock;

the first delay period having a duration sufficient to ensure that integrity of the first memory operation is not affected by the second memory operation and to ensure that the second time period overlaps the first time period such that the first and second memory operations are completed within the same test clock cycle of the test element.

2. The method as claimed in Claim 1, the access ports further including a third port, the test element further including a third memory operation that follows the second test element, wherein:

in step a), the test clock signals further include a third test clock for controlling memory access through the third port, clock pulses of the third test clock lagging corresponding clock pulses of the second test clock by a second delay period; and

in step b), the third memory operation is further conducted in the folded sequence upon said one of the memory cells during the same test clock cycle of the test element, wherein the third memory operation is conducted through the third port during a third time period starting from a leading edge of one of the clock pulses of the third test clock and ending at a lagging

edge of said one of the clock pulses of the third test clock;

the second delay period having a duration sufficient to ensure that integrity of the second memory operation is not affected by the third memory operation and to ensure that the third time period overlaps the second time period such that the first, second and third memory operations are completed within the same test clock cycle of the test element.

3. The method as claimed in Claim 1, wherein the test pattern is generated in accordance with a March algorithm.

4. The method as claimed in Claim 1, wherein each of the memory operations is one of a read 1 operation, a write 0 operation, a read 0 operation and a write 1 operation.

5. A computer program comprising program instructions for causing a testing apparatus to perform steps of a method of testing a multi-port memory in accordance with a test pattern, the memory including a set of access ports and a plurality of memory cells accessible through the access ports, the access ports including at least first and second ports, the test pattern including at least a test element that is to be performed upon each of the memory cells and that includes at least consecutive first and second memory operations, said method including:

a) generating a set of test clock signals that have the same test clock frequency, the test clock signals including at least a first test clock for controlling memory access through the first port, and a second test clock for controlling memory access through the second port, clock pulses of the second test clock lagging corresponding clock pulses of the first test clock by a first delay period; and

b) conducting the first and second memory operations in a folded sequence upon one of the memory cells during the same test clock cycle of the test element, wherein the first memory operation is conducted through the first port during a first time period starting from a leading edge of one of the clock pulses of the first test clock and ending at a lagging edge of said one of the clock pulses of the first test clock, and wherein the second memory operation is conducted through the second port during a second time period starting from a leading edge of one of the clock pulses of the second test clock and ending at a lagging edge of said one of the clock pulses of the second test clock;

the first delay period having a duration sufficient to ensure that integrity of the first memory operation is not affected by the second memory operation and to ensure that the second time period overlaps the first time period such that the first and second memory operations are completed within the same test clock cycle

of the test element.

6. The computer program as claimed in Claim 5, the access ports further including a third port, the test element further including a third memory operation that follows the second test element, wherein:

in step a), the test clock signals further include a third test clock for controlling memory access through the third port, clock pulses of the third test clock lagging corresponding clock pulses of the second test clock by a second delay period; and

in step b), the third memory operation is further conducted in the folded sequence upon said one of the memory cells during the same test clock cycle of the test element, wherein the third memory operation is conducted through the third port during a third time period starting from a leading edge of one of the clock pulses of the third test clock and ending at a lagging edge of said one of the clock pulses of the third test clock;

the second delay period having a duration sufficient to ensure that integrity of the second memory operation is not affected by the third memory operation and to ensure that the third time period overlaps the second time period such that the first, second and third memory operations are completed within the same test clock cycle of the test element.

7. The computer program as claimed in Claim 5, wherein the test pattern is generated in accordance with a March algorithm.

8. The computer program as claimed in Claim 5, wherein each of the memory operations is one of a read 1 operation, a write 0 operation, a read 0 operation and a write 1 operation.